Please replace the paragraph starting in Page 53, line 13 with the following amended paragraph.

FIG. 25 is a flowchart representation of a portion of a program, which may be running upon a secure memory socket or a secure memory device, in accordance with one embodiment of the present invention. Said program begins at **540** at which any required initialization is performed. The program continues to **541** at which boundaries of program memory addresses are compared to memory addresses placed upon program memory bus by a microprocessor executing instruction stored in said program memory. If, at **541**, address presented to the program memory is within predetermined high and low bounds, the program returns to compare next address presented to program memory to said predetermined high and low bounds. If, at **541**, address presented to the program memory is not within predetermined high and low bounds, the program continues to **542** at which access to program memory is disabled, and continues on to **543** at which a predetermined pattern is placed upon the program memory data bus. Effect of actions in **542** and **543** is to disable a microprocessor depending upon program memory for program instruction. Actions **542** and **543** maintain control device stability after disabling memory access by placing a disable pattern on the bus. Program continues to **544** at which a location in program memory is set to a predetermined state to indicate an error has occurred to a program calling the program described in **FIG. 25** and the program exits at **545**.